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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/697,311	10/31/2003	Yoshinori Shizuno	OHG 143	9864

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EXAMINER	
LEE, EUGENE	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 05/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

H:A

Office Action Summary	Application No.	Applicant(s)	
	10/697,311	SHIZUNO, YOSHINORI	
	Examiner	Art Unit	
	Eugene Lee	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *10-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Claims 10, and 11 were withdrawn in view of the applicant's election filed 9/20/05. However, upon allowance of any generic claims (claim 1 is generic), applicant will be entitled to consideration of claims to additional species which are written in dependent form (i.e. claims 10, and 11) or otherwise include all the limitations of an allowed generic claim as provided by 37 CFR 1.141.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1 thru 3, 5, and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamigawa et al. JPO 2000208556 A in view of Hirano et al. 6,472,749 B1. Nakamigawa discloses (see, for example, figure 3) a semiconductor device comprising a semiconductor chip 1, plurality of chip electrodes (plurality of electrode pads) 10, resin (extension portion) 9, adhesives (insulating film) 4, wirings (plurality of wiring patterns) 5, substrate (sealing portion) 2, and plurality of solder balls (plurality of external terminals) 12. Nakamigawa does not disclose the electrode pads being arranged in a first line extending in a first direction along a peripheral edge of the semiconductor chip on the first main surface, and the external terminals being arranged in a second line extending in a second direction perpendicular to said first direction, and being

electrically connected to the electrode pads in a one-on-one connection relationship. However, Hirano discloses (see, for example, FIG. 14) a semiconductor device comprising a semiconductor chip 7B, electrodes (electrode pads) 8, and bumps lands (external terminals) 4. The electrodes extend vertically on the peripheral edge of the semiconductor chip 7B, and connect to the bump lands, which extend horizontally, in a one-on-one relationship. It would have been obvious to one of ordinary skill in the art at the time of invention to have the electrode pads being arranged in a first line extending in a first direction along a peripheral edge of the semiconductor chip on the first main surface, and the external terminals being arranged in a second line extending in a second direction perpendicular to said first direction, and being electrically connected to the electrode pads in a one-on-one connection relationship in order to connect the chip externally in a manner which maximizes the area of a semiconductor device.

Regarding claims 2, and 3, see, for example, figure 3 wherein Nakamigawa discloses vertical regions (electrode posts) in between the solder ball 12 and the pad 13.

Regarding claims 5, and 6, it has been held that a recitation (i.e. formed as solders balls, lands) with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex Parte Masham, 2 USPQ F. 2d 1647 (1987).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamigawa et al. JP 2000208556 A in view of Hirano et al. '749 B1 as applied to claims 1-3, 5, and 6 above, and further in view of Jackson et al. 6,800,930 B2. Nakamigawa in view of Hirano does not disclose a thin oxidation layer formed on a side surface of said electrode posts. However, Jackson discloses (see, for example, Fig. 3) a semiconductor device comprising vias 124, conductive material 130, and dielectric layer (thin oxidation layer) 128. In column 6, lines 55-62, Jackson discloses the dielectric layer being silicon dioxide. It would have been obvious to one of ordinary skill in the art at the time of invention to have a thin oxidation layer formed on a side surface of said electrode posts in order to prevent diffusion of the vertical regions into other regions of the semiconductor device.

6. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamigawa et al. JP 2000208556 A in view of Hirano et al. '749 B1 as applied to claims 1-3, 5, and 6 above, and further in view of Torres et al. 5,898,213. Nakamigawa in view of Hirano does not disclose a portion of said wiring patterns on a boundary and a vicinity of a boundary between a region on the upper side of said semiconductor chip and said extension portion being formed wider or more thickly than other portions of said wiring patterns. However, Torres discloses (see, for example, FIG. 3) a semiconductor device comprising bonding posts 36 that are wider along a boundary A, and B. It would have been obvious to one of ordinary skill in the art at the time of invention to have a portion of said wiring patterns on a boundary and a vicinity of a boundary between a region on the upper side of said semiconductor chip and said extension portion being formed

wider or more thickly than other portions of said wiring patterns in order to form a staggered configuration that permits substantially more connections in the limited amount of space of the semiconductor device.

7. Claims 8, and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamigawa et al. JP 2000208556 A in view of Hirano et al. '749 B1 as applied to claims 1-3, 5, and 6 above, and further in view of Ma et al. 6,271,469 B1. Nakamigawa in view of Hirano does not disclose said extension portion being formed from a material having a greater molding shrinkage than the molding shrinkage of said sealing portion. However, Ma discloses (see, for example, FIG. 1K) a package comprising an encapsulating material (extension portion) 112, and first dielectric layer (sealing portion) 118. In column 3, lines 54-63, and column 4, lines 6-12, Ma discloses the encapsulating material comprising plastics, resins, and the first dielectric layer comprising silicon dioxide, silicon nitride. Plastics, resins have a greater molding shrinkage than silicon oxide, silicon nitride. Ma further discloses the encapsulation provides mechanical rigidity, protects the die from contaminants, and provides surface area for the build-up of trace layers. The first dielectric layer provides an adequate material so that vias may be formed thereon. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have said extension portion being formed from a material having a greater molding shrinkage than the molding shrinkage of said sealing portion in order to have an extension portion that has mechanical rigidity, protects the die from contaminants, and provides surface area for the build-up of trace layers, and a sealing portion made of a material that can support the wirings.

Regarding claim 9, Nakamigawa in view of Hirano in view of Ma does not disclose said extension portion having a linear expansion coefficient in a lower temperature range than glass transition temperature of less than 1.5.times.10.sup.-5/.degree. C. and a modulus of elasticity within a range of 7.8 to 22 GPa. However, it would have been obvious to one of ordinary skill in the art at the time of invention was made to use a material having a linear expansion coefficient in a lower temperature range than glass transition temperature of less than 1.5.times.10.sup.-5/.degree. C. and a modulus of elasticity within a range of 7.8 to 22 Gpa in order to have a material that has adequate mechanical rigidity, provides protection for the semiconductor chip, and provides surface area for the build-up of trace layers.

Response to Arguments

8. Applicant's arguments with respect to claims 1-9 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

INFORMATION ON HOW TO CONTACT THE USPTO

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eugene Lee whose telephone number is 571-272-1733. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on 571-272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Eugene Lee
April 19, 2006

EUGENE LEE
PRIMARY EXAMINER